

## CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor substrate assembly, comprising:  
providing at least one semiconductor die having a plurality of bond pads formed on an active surface thereof;  
attaching at least one anisotropically conductive layer comprising a plurality of laterally isolated conductive elements disposed in a dielectric material and having upper ends exposed therethrough to the active surface;  
forming a plurality of conductive bumps on the at least one anisotropically conductive layer with each conductive bump in contact with at least one conductive element of the plurality;  
and  
forming wire bonds between the bond pads and the conductive bumps.
2. The method of claim 1, further including forming the at least one anisotropically conductive layer to comprise conductive elements in the form of discrete metal columns embedded in a polymeric material.
3. The method of claim 2, further comprising forming the discrete metal columns to have a diameter of about 1  $\mu\text{m}$  to about 15  $\mu\text{m}$ .
4. The method of claim 2, further comprising forming the discrete metal columns to have a diameter of about 2  $\mu\text{m}$  to about 8  $\mu\text{m}$ .
5. The method of claim 2, further comprising forming the polymeric material as a tape or film.
6. The method of claim 1, further comprising forming the conductive elements of at least one of tungsten, aluminum, copper, silver, gold, and alloys thereof.

7. The method of claim 1, further including attaching the at least one anisotropically conductive layer to the active surface by an adhesive.

8. The method of claim 1, further comprising:  
placing the at least one semiconductor die on a substrate having a plurality of terminal pads on a surface thereof; and  
forming wire bonds between the plurality of conductive bumps and the plurality of terminal pads.

9. The method of claim 8, further comprising selecting the substrate to comprise one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

10. A method of claim 8, further comprising forming a dielectric layer over the at least one semiconductor die, the bond pads, the conductive bumps and the wire bonds.

11. The method of claim 1, further comprising attaching the conductive bumps to the conductive elements by at least one of high temperature, ultrasonic vibration and physical pressure.

12. The method of claim 1, wherein the conductive bumps are formed on the conductive elements and the wire bonds are formed by standoff stitch bonding.

13. The method of claim 1, further comprising forming the conductive bumps and the wire bonds of gold.

14. The method of claim 1, further comprising providing the at least one semiconductor die with the plurality of bond pads centrally located along an axis thereof and wherein attaching the at least one anisotropically conductive layer comprises attaching an anisotropically conductive layer adjacent the plurality of bond pads on opposing sides thereof.

15. The method of claim 14, wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice, and further comprising anisotropically conductive layers between pluralities of bond pads of adjacent dice and extending over boundaries therebetween.

16. The method of claim 15, further including singulating semiconductor dice from the wafer and severing the anisotropically conductive layers along the boundaries.

17. The method of claim 1, further including providing the at least one semiconductor die in the form of a singulated die, a partial wafer comprising a plurality of semiconductor dice or a wafer comprising a plurality of semiconductor dice.

18. The method of claim 17, wherein the at least one semiconductor die comprises a wafer, and further comprising severing a plurality of semiconductor dice from the wafer after forming wire bonds between the bond pads and the conductive bumps.

19. The method of claim 1, further comprising forming another plurality of conductive bumps on the plurality of conductive bumps.

20. The method of claim 19, further comprising:  
placing the at least one semiconductor die active surface down on a substrate having a plurality of terminal pads on a surface thereof with the conductive bumps of the another plurality in alignment with the terminal pads; and  
bonding the conductive bumps of the another plurality to the terminal pads.

21. The method of claim 20, further comprising selecting the substrate to comprise one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

22. The method of claim 20, wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice and the substrate comprises a wafer-scale

substrate, and further comprising singulating semiconductor dice from the wafer and segments from the wafer-scale substrate after the conductive bumps of the another plurality are bonded to the terminal pads.

23. The method of claim 20, further comprising introducing a dielectric underfill material between the at least one semiconductor die and the substrate.

24. The method of claim 19, further comprising covering the plurality of conductive bumps, the bond pads and the wire bonds therebetween with a dielectric material, leaving at least a portion of each of the conductive bumps of the another plurality exposed therethrough.

25. The method of claim 1, further comprising forming the conductive bumps and the wire bonds of gold.

26. A semiconductor substrate assembly, comprising:  
at least one semiconductor die having a plurality of bond pads formed on an active surface thereof;  
at least one anisotropically conductive layer comprising a plurality of laterally isolated conductive elements disposed in a dielectric material and having upper ends exposed therethrough attached to the active surface;  
a plurality of conductive bumps on the at least one anisotropically conductive layer with each conductive bump in contact with at least one conductive element of the plurality; and  
wire bonds between the bond pads and the conductive bumps.

27. The assembly of claim 26, wherein the at least one anisotropically conductive layer comprises conductive elements in the form of discrete metal columns embedded in a polymeric material.

28. The assembly of claim 27, wherein the discrete metal columns have a diameter of about 1  $\mu\text{m}$  to about 15  $\mu\text{m}$ .

29. The assembly of claim 27, wherein the discrete metal columns have a diameter of about 2  $\mu\text{m}$  to about 8  $\mu\text{m}$ .

30. The assembly of claim 27, wherein the polymeric material comprises a tape or film.

31. The assembly of claim 26, wherein the conductive elements comprise at least one of tungsten, aluminum, copper, silver, gold, and alloys thereof.

32. The assembly of claim 26, wherein the at least one anisotropically conductive layer is attached to the active surface by an adhesive.

33. The assembly of claim 26, further comprising:  
a substrate having a plurality of terminal pads on a surface thereof; and  
wire bonds between the plurality of conductive bumps and the plurality of terminal pads.

34. The assembly of claim 33, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

35. The assembly of claim 32, further comprising a dielectric layer over the at least one semiconductor die, the bond pads, the conductive bumps and the wire bonds.

36. The assembly of claim 26, wherein the conductive bumps are attached to the conductive elements by metallurgical bonds.

37. The assembly of claim 26, wherein the conductive bumps and the wire bonds are formed of gold.

38. The assembly of claim 26, wherein the at least one semiconductor die has the plurality of bond pads centrally located along an axis thereof and the at least one anisotropically conductive layer comprises a plurality of anisotropically conductive layers adjacent the plurality of bond pads on opposing sides thereof.

39. The assembly of claim 38, wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice, and the plurality of anisotropically conductive layers are disposed between pluralities of bond pads of adjacent semiconductor dice and extending over boundaries therebetween.

40. The assembly of claim 26, wherein the at least one semiconductor die is in the form of a singulated die, a partial wafer comprising a plurality of semiconductor dice or a wafer comprising a plurality of semiconductor dice.

41. The assembly of claim 26, further comprising another plurality of conductive bumps, each conductive bump of the another plurality disposed on one of the plurality of conductive bumps.

42. The assembly of claim 41, further comprising:  
a substrate having a plurality of terminal pads on a surface thereof with the conductive bumps of the another plurality in alignment with and bonded to the terminal pads.

43. The assembly of claim 42, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

44. The assembly of claim 43, wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice and the substrate comprises a wafer-scale substrate.

45. The assembly of claim 42, further comprising a dielectric underfill material between the at least one semiconductor die and the substrate.

46. The assembly of claim 41, further comprising a dielectric material covering the plurality of conductive bumps, the bond pads and the wire bonds therebetween and leaving at least a portion of each of the conductive bumps of the another plurality exposed therethrough.